ZnO SINGLE BARRIER VARISTOR FOR LOGIC CIRCUITS PROTECTION

PROGRESS REPORT

Prepared for

Harry Diamond Laboratories

Contract DAALO2 - 91 - 0040

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International Technology Services, Inc.

Development of ZnO Single Barrier Varistor under this SBIR program has shown very promising results. The pure ZnO used as a substrate for forming the single barrier varistor was prepared by pressing pure (99.99%) polycrystalline ZnO powder and then sintering at 1550° C in air. The as-sintered samples are disks shapes of 2.5 cm diameter and 2 - 4 mm thickness. The density after high temperature sintering is 5.4 - 5.6 gm / cc (~ 95 - 99 % of theoretical density) .

Current voltage measurements of the pure as-sintered ZnO disks show very high resistivity at room temperature. As-sintered specimens were almost insulators. In order to make them more conductive we added some alumina oxide powder to the original polycrystalline ZnO mixed and sintered using the same conditions.

After polishing with 0.6 µm alumina powder the surface of ZnO was covered with the bismuth oxide powder and was heat treated at different temperatures from 860° C to 1160° C for 30 - 60 mins in air. Then the rest of the bismuth oxide had been removed from the surface by polishing, and silver contacts were applied on the top and the bottom of the specimen for I - V measurements.

The obtained structure of ZnO varistor was examined on the SEM. The I - V characteristics of all the specimens had been taken by using two coordinate recorder.

The results obtained showed a non-linear I - V characteristics with the breakdown voltage 4.5 - 6.5 volts. The I - V curves are reproducible and displayed varistor's behavior for both positive and negative bias. The nonlinearity coefficient was calculated to be 10 - 15. However, it is expected when the series resistance of the bulk ZnO is subtracted a much higher nonlinearity coefficient will result. The bulk resistivity of as-sintered ZnO was obtained using 4-points measurements.

Effect of annealing temperature and ambient temperature on the device stability is currently being investigated. It has been already found that devices annealed at high temperature ~~of~~ for a long time became almost insulators.

The analysis of the tested samples on the SEM displayed significant difference in the penetration depth and its character for the samples annealed at different temperatures and times. We are continuing to study the structure of the obtained varistors on the SEM.

The X-ray diffraction data of annealed specimens showed that during annealing the new phase had been formed - 24 Bi_2O_3 * ZnO. The new phase formed the grain boundary interface and ZnO grains of the doped layer are surrounded by this new phase.

The achievement of nonlinearity at this low threshold voltage 4.5 - 6.5 volts show a great promise to obtain low voltage varistors. The technique used is compatible with IC processing and can be produced at low cost for logic circuits protection application.

We are currently conducting more experimental runs to optimize the *process and check device stability and reliability.*

Further analysis of the results and modeling is under development and final report.

F. A. Selim

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LIST OF FIGURES

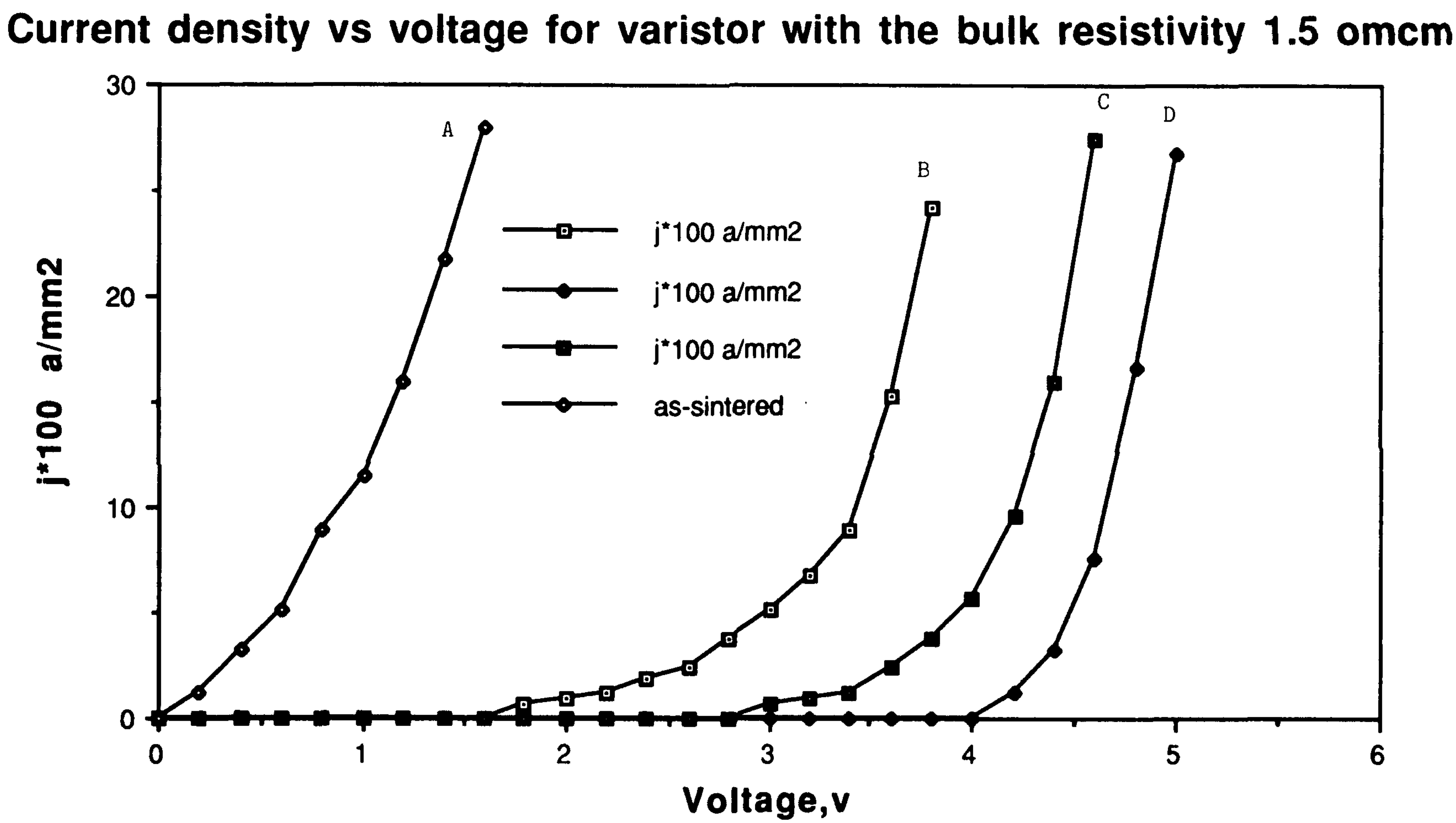
Current density vs voltage for varistor with the bulk resistivity 1.5 omcm
j*100 a/mm2
Voltage,v
0
10
20
30
0
1
2
3
4
5
6
A
B
C
D
j*100 a/mm2
j*100 a/mm2
j*100 a/mm2
as-sintered

Fig. 1

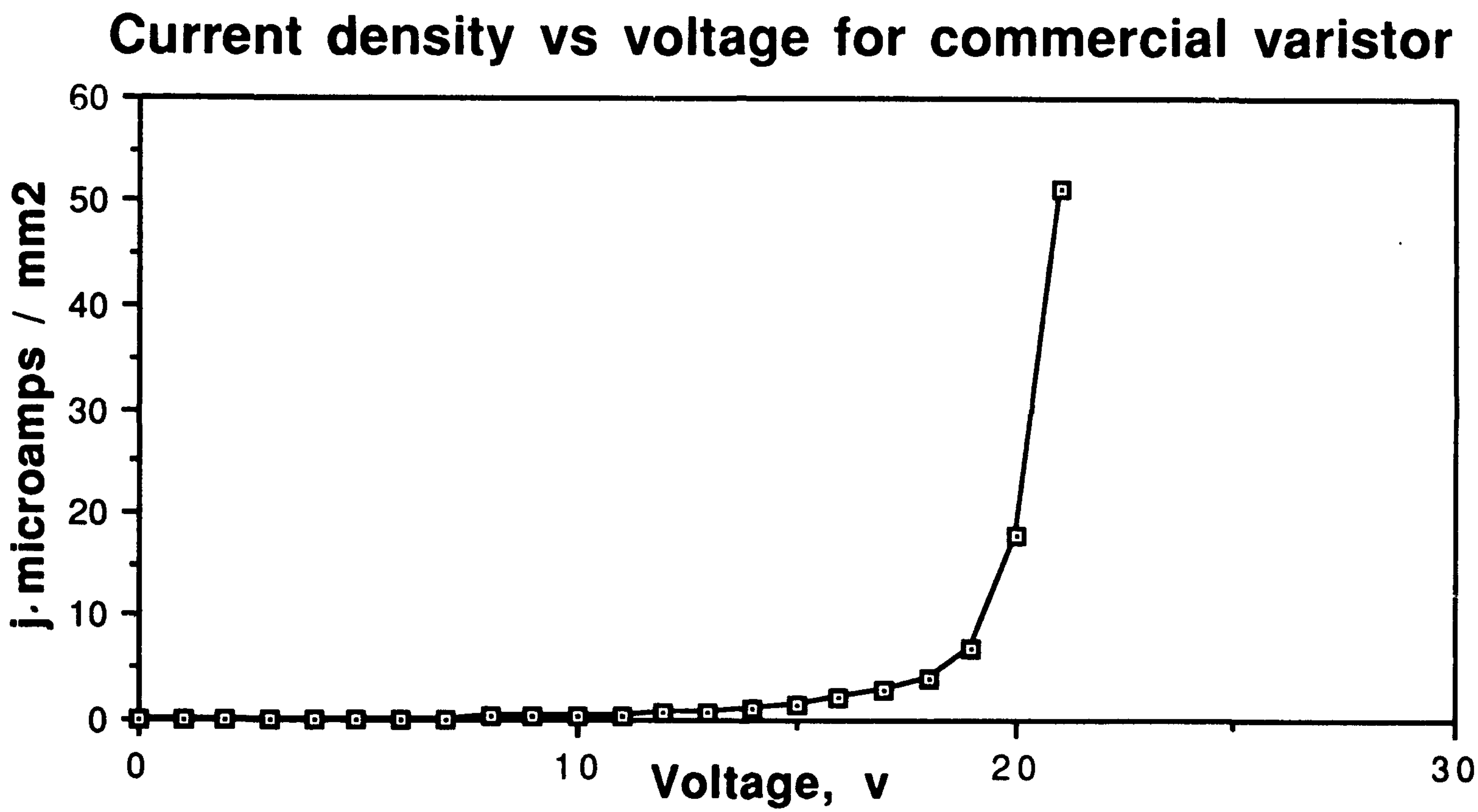
Current density vs voltage for commercial varistor
j·microamps / mm2
60
50
40
30
20
10
0
0
10
20
30
Voltage, v

Fig. 2

A90-330

Low Voltage ZnO Single Barrier Varistors for Logic Circuits

Protection (3-V) and Commercial Applications (12V)

International Technology Services, Inc.

II

The feasibility of producing ZnO varistors with low voltage (3-5V) and high non-linearity co-efficient of 24-40 for IC protection from electrical transients has been demonstrated under this SBIR Phase I program. The devices are processed by forming single barrier junctions through diffusion of Bi and other impurities into pure ZnO wafers. The technique used is compatible with IC processing and can be used to produce low cost devices for logic circuit protection.

The success of Phase I paves the way for Phase II which has the objective of demonstrating the manufacturibility of low cost varistors with stable I-V characteristics and fast response time. The voltage application will be extended from (3-12 V) for dual use. This phase will involve process optimization, characterization, impedance measurements, surge and frequency response measurements up to 100 MHz, device stability at different operating temperatures up to 125° C, device surface passivation, leakage current control, and high energy handling capability for testing in protection of the advanced state-of-the-art integrated circuits including VHSICS and MIMICS, and for higher voltage (= 12 V) application.

Phase II plan is comprised of three basic stages: i.e. (1). A Basic Effort to study feasibility and of devices up to 10 MHZ application. (2). Option 1 Effort to extend application up to 100 MHz and (3). Option 2 effort to study device optimization and study limitation to higher frequency application, and processing packaging for commercial applications.

The concept proposed is anticipated to yield low cost rugged commercial devices. The end-users who will benefit from this product include all those utilizing low-voltage, low power transients e.g. telecommunication systems, automotive electronic systems and computers.

Zinc Oxide	Varistors
Current	Impedance
Voltage	Transient
Frequency	Integrated Circuits

I. Background, Identification of the Problem, and Opportunity

Recent advances in integrated circuit technology have resulted in low voltage, low power consumption chips which require low voltage surface mounted protection form electrical transients. The most suitable candidate for this application is the Metal Oxide Varistor (MOV). An MOV, small in dimensions (0.5mm x 1mm x 1.5mm), having breakdown voltages in the range of 3 to 12 V and non-linear co-efficients from 25 to 50 is required for this purpose.

Although commercial MOV's with such high non-linearity co-efficients e.g. ZnO varistors, have been available they are mainly rated for high voltage circuit protection in the KV range. ZnO varistors have superior nonlinear current-voltage characteristics over SiC, Se, etc. devices. These varistors are ceramic devices produced by sintering mixtures of ZnO powder with other oxides such as Bi_2O_3, Sb_2O_3, Co_3O_4, MnO_4, CrO_2O_3. These devices yield a non-linear current-voltage (I-V) characteristic as expressed by the relation $I = K V^n$, where K is a constant and n is a non-linearity coefficient dependent on the microstructure of the devices (1,2). The microstructure is generally believed to consist of ZnO grains surrounded by thin insulating metal-oxide barriers (3-6), but some studies show that the intergranular layer is absent in the vast majority of grain-to-grain boundaries (7). The blocking voltage V in these devices can be written as V = Ng Vg, where Ng is the number of grains in series within a device and Vg is the voltage per grain which is estimated to be 2-4 volts in commercially available ZnO varistors (8-12). The number of

grains Ng is related to the thickness of ZnO sample t by the relation Ng = t/lg, where lg is the grain size (10-20 micron in a typical device). Therefore, for low voltage applications (e.g. 3-12 volts) at a given current, the thickness of the device becomes very small (10-100 micron) as seen from the above relations.

Because energy absorption is proportional to volume, this means that lowering the voltage and hence the thickness requires a large diameter to achieve the same energy absorption rating needed for circuit protection. Thin, large diameter discs are difficult to assemble without breaking, even if they can be made (e.g. by lapping). Moreover, they are not compatible with the corresponding shrinking of IC circuit geometries. In addition, non-uniformities in the microstructure of thin devices will play a larger role in determining the current distribution and will make the device more susceptible to current crowding and hot spots. Although low voltage devices can be made by increasing the grain size, this requires much higher temperature and longer processing time.

In Phase I we presented an alternate method for making low voltage devices without the necessity for making thin large-area discs, or discs of very large grain size. The method consists of alloying Bi from the surface into a pure ZnO substrate. This process forms a single barrier junction which results in low voltage varistor characteristics (9). This single barrier approach allows one to achieve any desired voltage by stacking metallized discs which can be packaged in a low-cost non-hermetic package.

Another advantage of the proposed structure is the ability to remove heat by placing a heat sink close to each cell. The energy absorption requirements can be met by adjusting

the disc thickness. Unlike a conventional ZnO varistor, there is no corresponding change in the breakdown voltage. Moreover, it is not necessary to use single crystal ZnO since the barriers within the poly-ZnO disc are low resistance in nature.

II. Summary of Research Work Carried Out in Phase I

The feasibility of producing low voltage ZnO MOV's with high non-linearity was demonstrated in Phase I. Fabrication and evaluation of ZnO single barrier devices were performed.

The polycrystalline ZnO devices were made as follows: Reagent grade Fisher ZnO powder with particle size less than 1 micron was milled in a urethane-lined ball mill using methyl alcohol binder (~50 wt. %). The powder was dried and granulated through mesh screen for uniform size selection. The material was pressed in a die at 60 MPa to a cylindrical shape 2.5 cm in diameter and 2-4 mm in thickness. Pressing was followed by sintering at 1400° C for 1.2 hours in air. Density after sintering was measured to determine porosity and effect of pressing pressure and sintering temperature in order to detect shrinkage and dimensional changes during subsequent annealing. The effect of sintering temperature and ambient on device characteristics was determined. The electrical resistivity of the pure ZnO bulk was measured. This resistivity represents the series resistance due to the ZnO bulk resistivity. It could be decreased by increasing the conductivity of ZnO grains during the course of sintering. This was accomplished by

doping the ZnO bulk with Al_2O_3 (0.3-1% wt). Ideally, the bulk resistivity should be minimum. The effect of processing parameters on bulk properties are presented in Section III.

Following wafer surface polishing, with ~0.6 micron alumina powder, the single barrier was formed using the following two methods. In the first method we coated the surface of the ZnO wafer using sputtering of a mixture containing the metal oxides of Bi, Sb, Cr, Mn, Co by sputtering to a thickness of 1000 to 2000 °A. This method was abandoned after it revealed linear I-V characteristics. In the second method Bi_2O_3 was alloyed directly on the ZnO surface. The single barrier was alloyed directly on the ZnO surface with Bi_2O_3 powder then the structure was heat-treated at different temperatures (860 - 1160° C) for 30 - 60 minutes in air. The annealing conditions were controlled in such a way that the diffusion distance would not exceed the length of the grain, although it is expected that there would be a relatively greater diffusion along the grain boundary. Diffusion along the grain boundaries which are parallel to the flow of current should not be of any concern for the present structure. Only the doped region will act as a barrier; the rest of the ZnO grain is a conductor. The devices were annealed in air, as we have found in earlier studies (8), that air annealing was important to obtain the non-linear characteristics.

After heat treatment, to form the single barrier using Bi *diffusion*, Bi_2O_3 was removed from the surface by polishing. Ag contacts were then applied on both sides of the structure to form electrodes. The obtained structure was examined using SEM and x-

ray diffraction.

The I-V characteristics were measured using two-coordinate recorder for I-V point-by-point readings. The Log I-Log V plots were used to calculate the non-linearity coefficient (n) from the empirical relation $I = KV^n$. The resistance (1/K) was calculated or measured. This resistance is a function of the bulk grain size which depends on the processing parameters. The non-linearity coefficient was measured between voltages of 10^2 to 10 volts and current densities of 3×10^{-3} A/mm^2 to 3×10^{-1} A/mm^2. n was compared with values of 25 to 100 of commercial high voltage varistors reported in literature (13-16). The non-linearity coefficient was calculated from I-V measurements of devices over the temperature range of 25 of 75° C to examine the effect of device operating temperature on n.

Low voltage varistors processed with this single barrier technique was analyzed as a function of field stress, time and temperature. We have found in our earlier attempt (9) that although some single barrier devices yield low threshold voltage (20V) they had a low non-linearity coefficient n (15) and a *shift (instability)* in the I-V characteristics with increased field and time. This effect was attributed to trapping of electrons from the ZnO semiconductor into the oxide layer. This was observed in the structured using sputtered oxide layers at the surface of the ZnO.

III. Summary of Phase I Results

The density of the sintered ZnO samples was 5.4 - 5.6 g/cm^3 (95 - 99% of theoretical density). Resistivity measurements of the as-sintered pure ZnO discs showed very high bulk resistivity (10 - 100 ohm-cm). Addition of Al_2O_3 powder to the pure ZnO powder before sintering resulted in a much higher conductivity. The conductivity was found to increase with the increase of Al_2O_3 doping. Resistivity of the as-sintered Al_2O_3-doped ZnO was 1.5 ohm-cm to 4.7 ohm-cm for 0.3 to 1.0% (weight) Al_2O_3 content, respectively.

I-V results for devices before and after junction formation for ZnO samples with 1.5 ohm-cm bulk resistivity is shown in Figure 1(a). Curve A shows a linear I-V characteristics and high resistivity of the as-sintered sample (before junction formation using Bi_2O_3 source). Curves B and C are two different devices after junction formation using Bi_2O_3 alloying and annealing in air at 860° C for 35 minutes. The devices show non-linear I-V characteristics with a threshold voltage of 3 to 5 volts. I-V characteristics for devices annealed under same conditions but having higher bulk resistivity (4.3 ohm-cm) are shown in Figure 1(b).

The non-linearity coefficient was calculated from the log I-log V relationship. A typical n value calculated between voltages of 10^{-2} to 10 V and current densities of 3 x 10^{-3} A/mm^2 to 0.3 A/mm^2 is 25. However, when the series voltage drop due to the series resistance of the bulk was subtracted, typical non-linearity co-efficients reaching 40 were

obtained. The threshold voltage of 3-5 volts is in good agreement with the 2 to 4 volts reported in literature for the "voltage per grain" values of commercial devices (13-15).

Figure 2 shows the symmetric I-V characteristics showing varistor behavior for positive and negative polarities for the devices of Figures 1(a) and(b). This represents a back-to-back Schottky diode characteristics i.e. a single barrier varistor. The structure represents a single grain of varistor as verified by SEM and x-ray measurement. To check the single-barrier theory, the Bi diffused surface layer was removed by polishing. When 80 micron of the surface was removed and the I-V were measured again, the non-linearity characteristics disappeared. This was also confirmed by measuring the grain size to be ~20 micron.

The effect of annealing temperature and time on varistor characteristics is shown in Figures 3 and 4. Figure 3 shows I-V characteristics of Bi_2O_3 diffused and annealed at 860° C for different times. The threshold voltage is shown to increase from 4 to 30 volts upon increasing the time from 30 to 60 minutes. This is expected as the diffusion increased to dope several grains of the ZnO bulk with Bi and forms more barriers contributing to the varistor behavior. The threshold voltage of 30 volts corresponds to a diffusion depth which was verified by x-ray and SEM measurements. This also confirms a breakdown voltage of 3 volts/grain. The same effect is shown in Figure 4 when the annealing temperature was increased to 1155° C. A much higher breakdown voltage results are obtained for higher annealing temperature as expected.

Device stability was examined by measuring the I-V characteristics at different

operating temperatures. Figure 5 shows the shift in the threshold voltage from a breakdown voltage of 4 to 1 as the operating temperatures is increased from room temperature measurement to 72° C. This shift in current-voltage characteristic was recovered when temperature stress was removed. This indicates a surface charge drift with temperature. Surface charge control can be achieved by surface passivation and packaging which will be addressed in this phase, (Phase II).

IV. Phase II Research Objectives

The objective of Phase II is to demonstrate the **manufacturability of dual use low voltage i.e. (3-12 V)** high non-linearity ZnO varistors with stable I-V characteristics and fast response time. Emphasis will involve process optimization, characterization, and device surface passivation for testing in protection of the advanced state-of-the-art integrated circuits including VHSICS and MIMICS, and commercial applications.

In Phase II, processing, characterization, and optimization of single barrier low voltage varistor will be carried out. The I-V characteristics, voltage breakdown, non-linearity coefficients, impedance and turn on **speed up to 100 MHz frequency** measurements, effect of annealing temperature and atmosphere on stability of device characteristics and reproductibility will be demonstrated.

V. Phase II Work Plan

The material composition and fabrication processing are, of course, the most important factors affecting the properties of ZnO varistors. Ideal ZnO varistors should have a microstructure characterized by a low-resistivity grain, high resistivity grain boundary barrier, and a uniformity in the size of ZnO grains. In conventional sintered ZnO devices, grains determine the threshold voltage per unit thickness and have a role as a heat sink for surge energy absorption. Our concept demonstrated in phase I eliminates the dependence of threshold voltage on grain size and on the variation in multi-grain boundary barrier system. The threshold voltage in our proposed device depends on the single barrier formed. This single barrier can be controlled independent of the ZnO body. Using this concept, the work to be accomplished in phase II consists of applied research and development of low voltage surface-mounted ZnO varistors for IC and commercial components protection from electrical transients. Material preparation, device processing and characterization, and studies of device reliability performance will be performed to examine the manufacturability and application of the proposed concept. The work plan includes theoretical, analytical and experimental investigation, and fabrication of a set of devices. The delivery of quarterly reports and a final report will constitute demonstration of the concept.

In Phase II, ITS, Inc. will perform the specific tasks defined below in fulfillment of the proposed program.

Specific Tasks

1) Fabrication of ZnO Polycrystalling Body. The polycrystalline ZnO proposed for this program will be made as outlined in Phase I. Reagent grade Fisher ZnO powder will be milled for a specified time in a urethane-lined ball mill using methyl alcohol binder (~ 50 wt.%). The powder will be dried and granulated through mesh screen for uniform size selection. The material will be pressed in a die at 60 MPa to the desired shape for future slicing to a wafer size determined by the configuration for packaging and surface mounting. Pressing will be following by sintering at temperatures from 800 to 1300 °C for 6 hours in air. Density after sintering will be measured to determine porosity and effect of pressing pressure and sintering temperature in order to detect shrinkage and dimensional changes during subsequent annealing. The effect of sintering temperature and ambient on device characteristics will be determined. The electrical resistivity of the pure ZnO bulk will be measured. This resistivity represents the series resistance due to the ZnO bulk resistivity. It could be decreased by increasing the conductivity of ZnO grains during the course of sintering and by A1 doping. Ideally, the bulk resistivity should be minimum. The effect of processing parameters on bulk properties will be examined.

2) Single Barrier Formation. ZnO discs will be sliced from the sintered boule to different slices varying from 1 to 3 mm thickness to study the contribution of the bulk ZnO in the I-V characteristics. The pure ZnO wafer should yield a linear

behavior in the absence of the oxide barriers. Following wafer surface polishing with ~ 1 micron diamond paste, the single barrier will be formed by the method demonstrated in phase I. We will coat the surface of the ZnO wafer with the metal oxide of Bi, followed by heat treatment at 860 - 1000° C in air for 30 - 60 minutes. The annealing conditions will be controlled in such a way that the diffusion distance would not exceed the length of the grain or grains required to achieve the desired voltage (3 - 12V), although it is expected that there would be a relatively greater diffusion along the grain boundary. Diffusion along the grain boundaries which are parallel to the flow of current should not be of any concern for the present structure. Only the doped region will act as a barrier; the rest of the ZnO grains is a conductor. The devices will be annealed in air, as we have found in our earlier studies (8), that air annealing was important to obtain the non-linear characteristics. Annealing will be performed under gas pressures of the oxides in order to eliminate any change in stoichiometry. Liquid In-Ga alloy or Ag contacts will then be applied on both sides of the structure to form electrodes.

3) Role of Additives: The addition of Bi_2O_3 to the original ZnO body has been found to be essential to yield the non-linearity behavior of varistors. A addition of transition oxides such as Co_3O_4 and MnO_2 also increase the non-linearity. Similarly, multiple dopants such as combination of Bi_2O_3, Co_3O_4, SiO_2, MnO_2, etc., produced greater non-linearity than that by a single dopant. To study the effect of different oxides on the non-linearity of varistors, the as-sintered ZnO samples

will be annealed with mixtures of different oxides on the surface, and I-V characteristics of the devices will be measured.

To form more uniform doped layers the devices will be annealed with the mixtures of different oxides at lower temperature (about 800° C) for longer periods of time.

Also, the reproductibility of I-V characteristics for the devices annealed with the mixtures of different oxides will be studied as a function of annealing temperatures and times.

4) Device Testing and Evaluation. The I-V measurements will be recorded from a curve tracer and I-V point-by-point readings, the log I-log V plots will be used to calculate the non-linearity coefficient (n) from the empirical relation $I = K V^n$. The resistance ~ (1/K) will be calculated. This resistance is a function of the bulk grain size which depends on the processing parameter. The non-linearity coefficient will be measured between voltages of 10^{-2} to 10^{2} volts and current densities of 10^{-5} to 10^{-4} A/mm^2 for the different methods of fabrication discussed above. n will be compared with values of 25 to 100 of commercial high voltage varistors reported in literature (13 - 15). The non-linearity coefficient will be calculated from I-V measurements of devices over the temperature range of 25 to 75° C to examine the effect of device operating temperature on n.

The measurements of leakage current through the varistor is important because of the amount of watt-loss at steady-state operating voltage. It also

determines the magnitude of the steady-state voltage at which the varistor can operate without generating an excessive amount of heat.

The leakage current will be measured as a function of annealing temperature and time and also as a result of annealing with the mixture of different oxides.

The time delay between input and output signals is an important characteristic of the varistor. The shorter the time delay the faster the varistor responds at the external voltage. The time shift is determined by the parameters of the doped layer (thickness, uniformity) and also by the conductivity of the bulk.

AC impedance measurements will be carried out to determine the time response for the low voltage ZnO varistor in the frequency range up to 100 MHz. The effect of processing parameters (temperature and time of annealing) on time response will be investigated. Preliminary measurements of phase shift and AC impedance as a function of frequency are shown in Figs. 6, 7, and 8.

A summary of the device fabrication and testing is shown in Table 1.

5) <u>Device Stability, Reliability and Process Optimization.</u> Low voltage varistors with single barrier junction technique will be analyzed as a function of field stress, time and temperature. We have found in our earlier attempt (9) that although some single barrier devices yielded low threshold voltage, they had a low non-linearity coefficient n (~15) and a shift (instability) in the I-V characteristics with increased field and time. This effect is attributed to trapping of electrons from the ZnO semiconductor into the oxide layer. This was observed in the structure using sputtered

oxide layers at the surface of the ZnO. This phenomenon can be eliminated by etching and cleaning the ZnO) varistor structure before applying the ohmic contacts. Results of the different structures proposed in this study will be compared in order to understand the conduction mechanism and optimize the device process for maximum n and the required threshold voltage V.

6) Surface Passivation and Device Packaging.

7) Delivery of Experimental Devices, Quarterly Reports and Final Technical Report. Results of this proposed work will be presented to demonstrate the feasibility of fabricating low voltage ZnO varistors with the desired n values of 25 to 50 and the reliability required for protection of integrated circuits and commercial circuits.

A schedule and a milestone chart of the project is shown in Table 2.

VI. References

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List of Figures

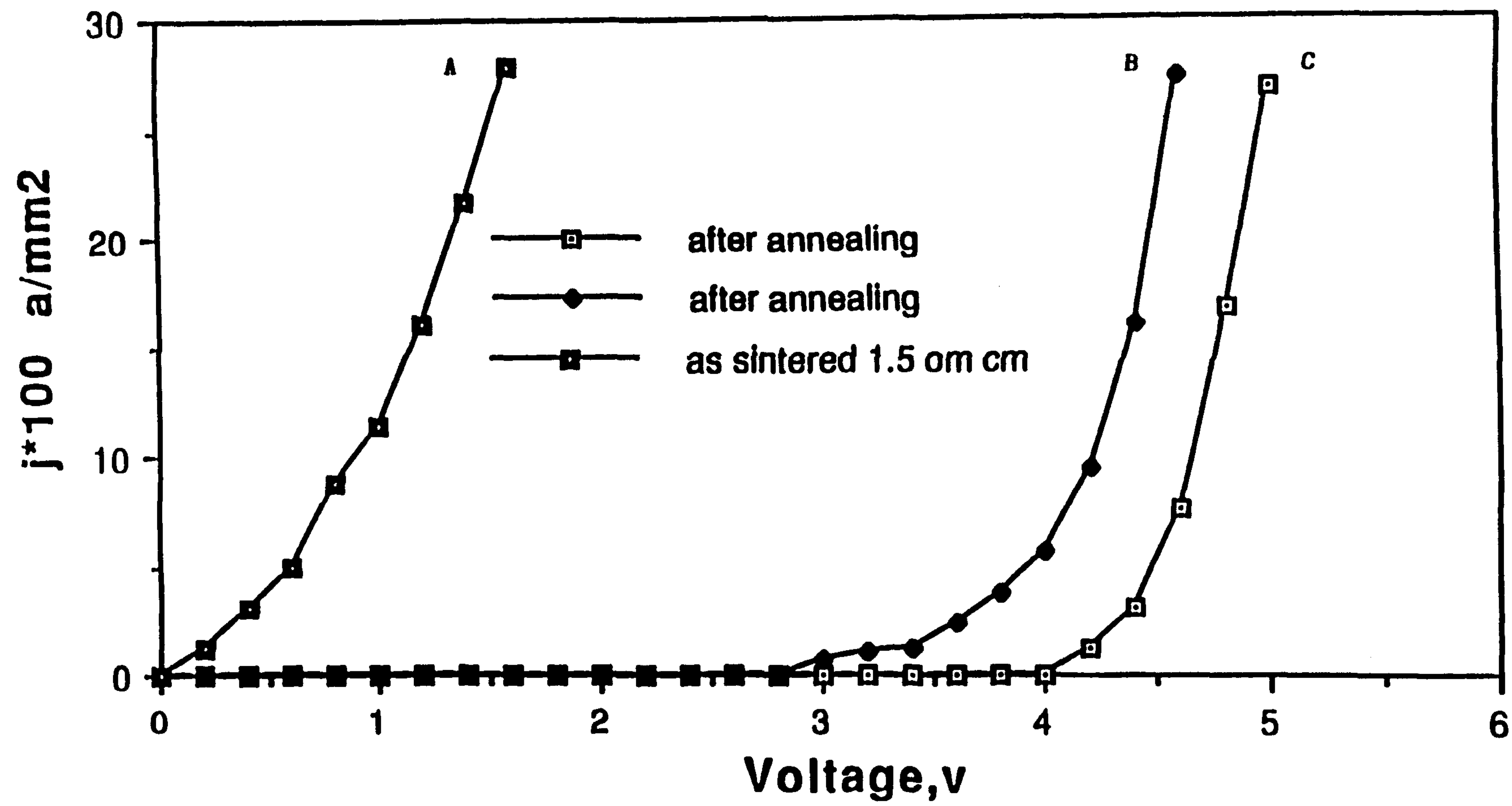
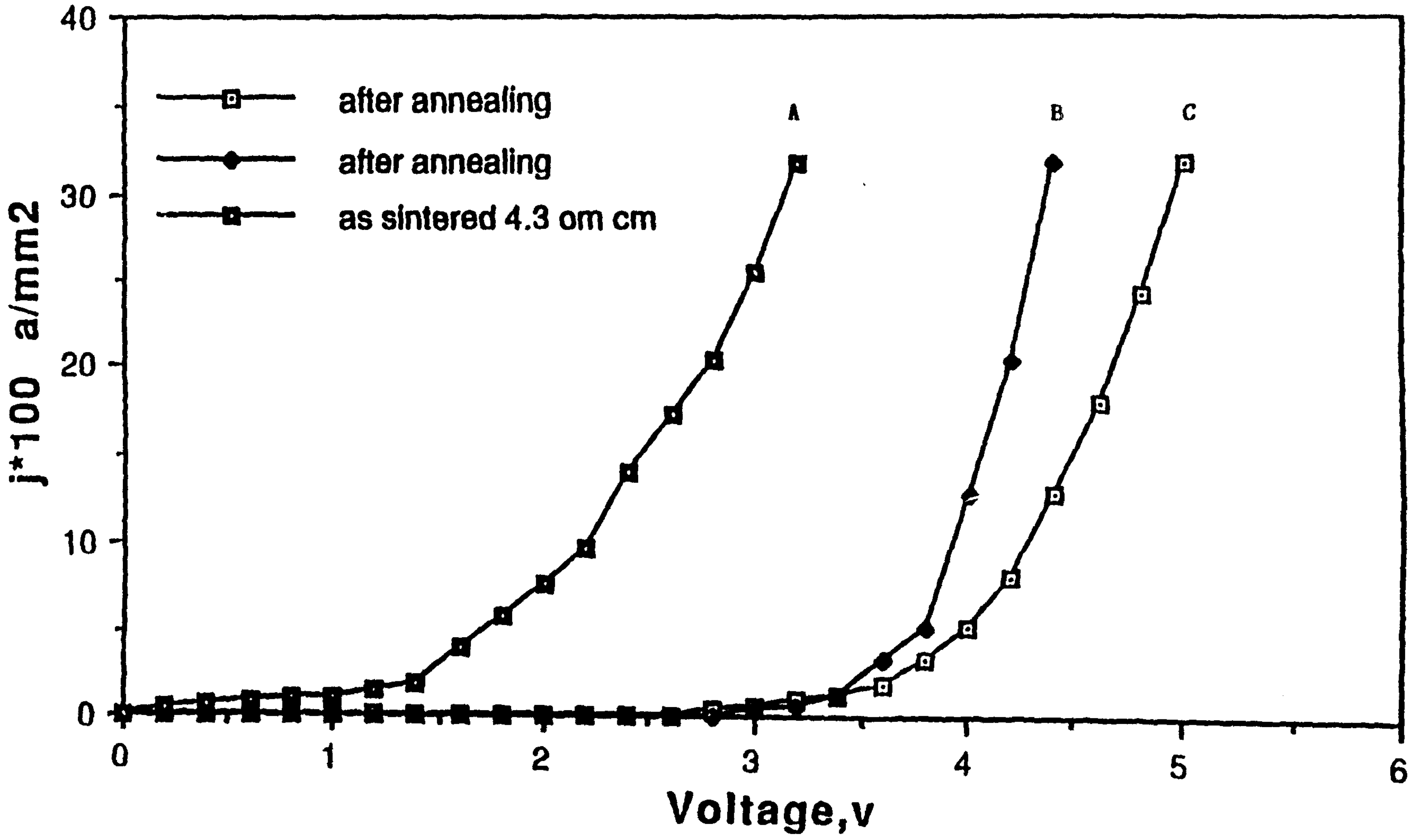

30
20
10
0
j*100 a/mm2
A
B
C
after annealing
after annealing
as sintered 1.5 om cm
0
1
2
3
4
5
6
Voltage,v

Figure 1(a)



after annealing
after annealing
as sintered 4.3 om cm
A
B
C
j*100 a/mm2
Voltage,v
0
10
20
30
40
0
1
2
3
4
5
6

Figure 1 (b)

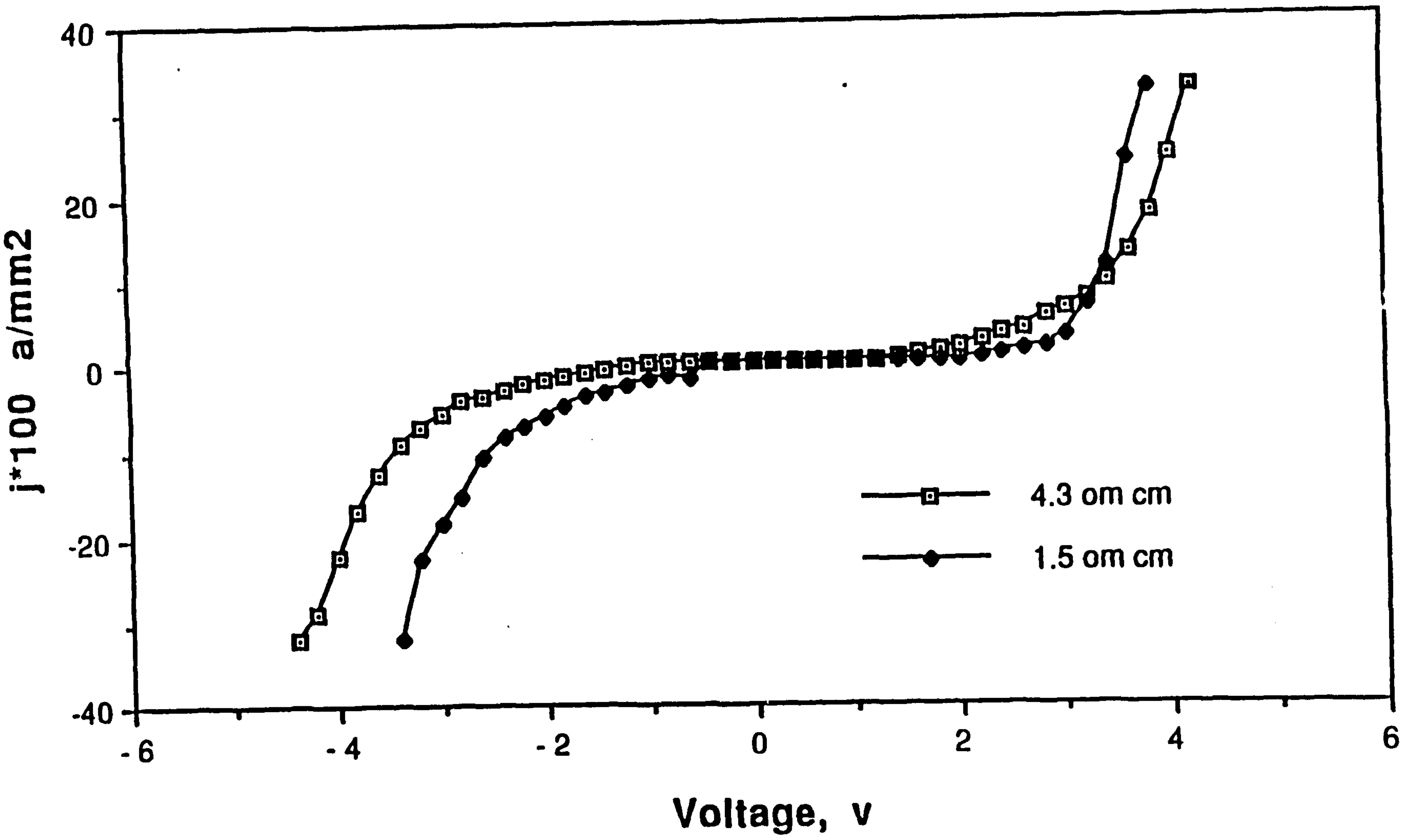
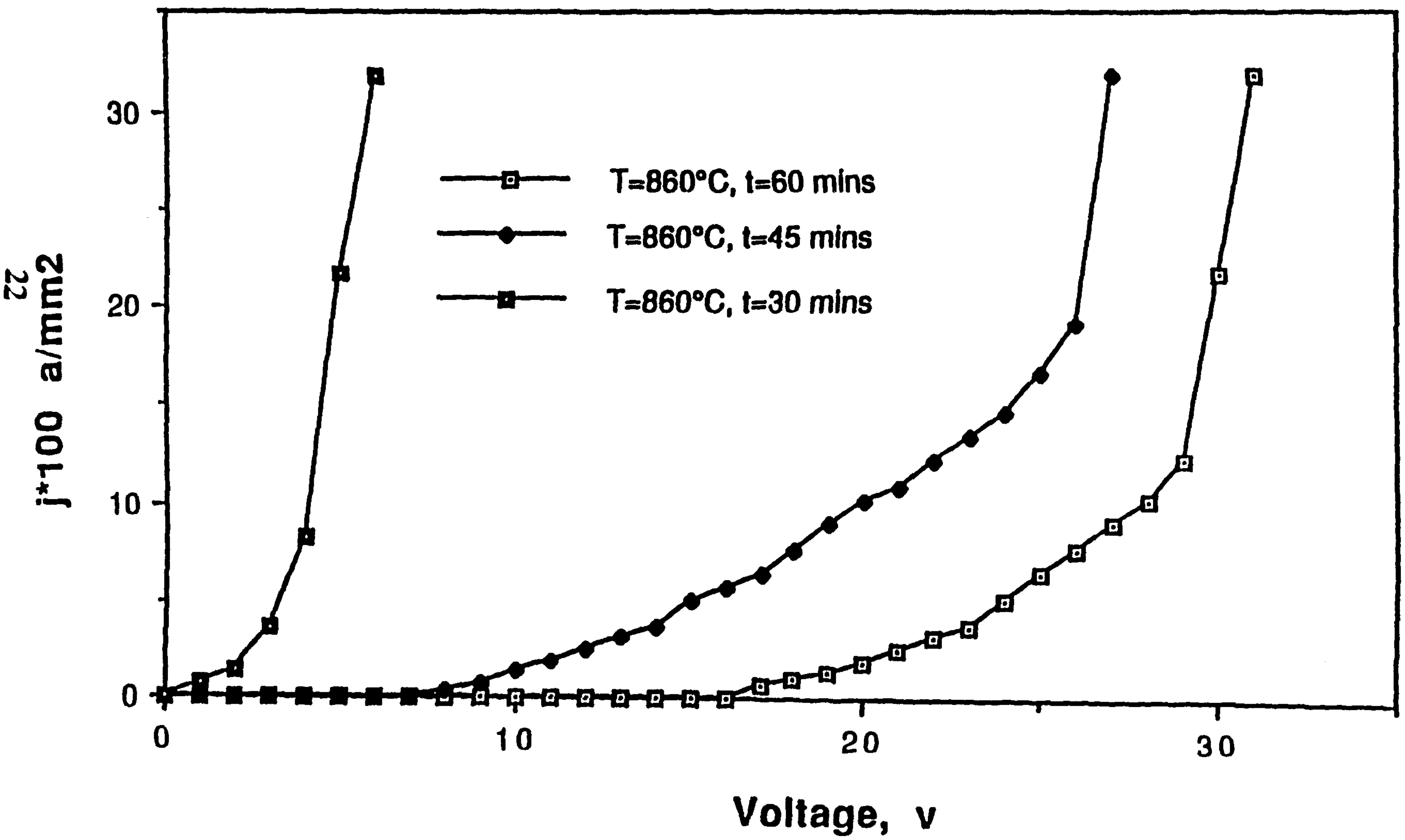


Figure 2



T=860°C, t=60 mins
T=860°C, t=45 mins
T=860°C, t=30 mins
j*100 a/mm2
Voltage, v
0
10
20
30

Figure 3

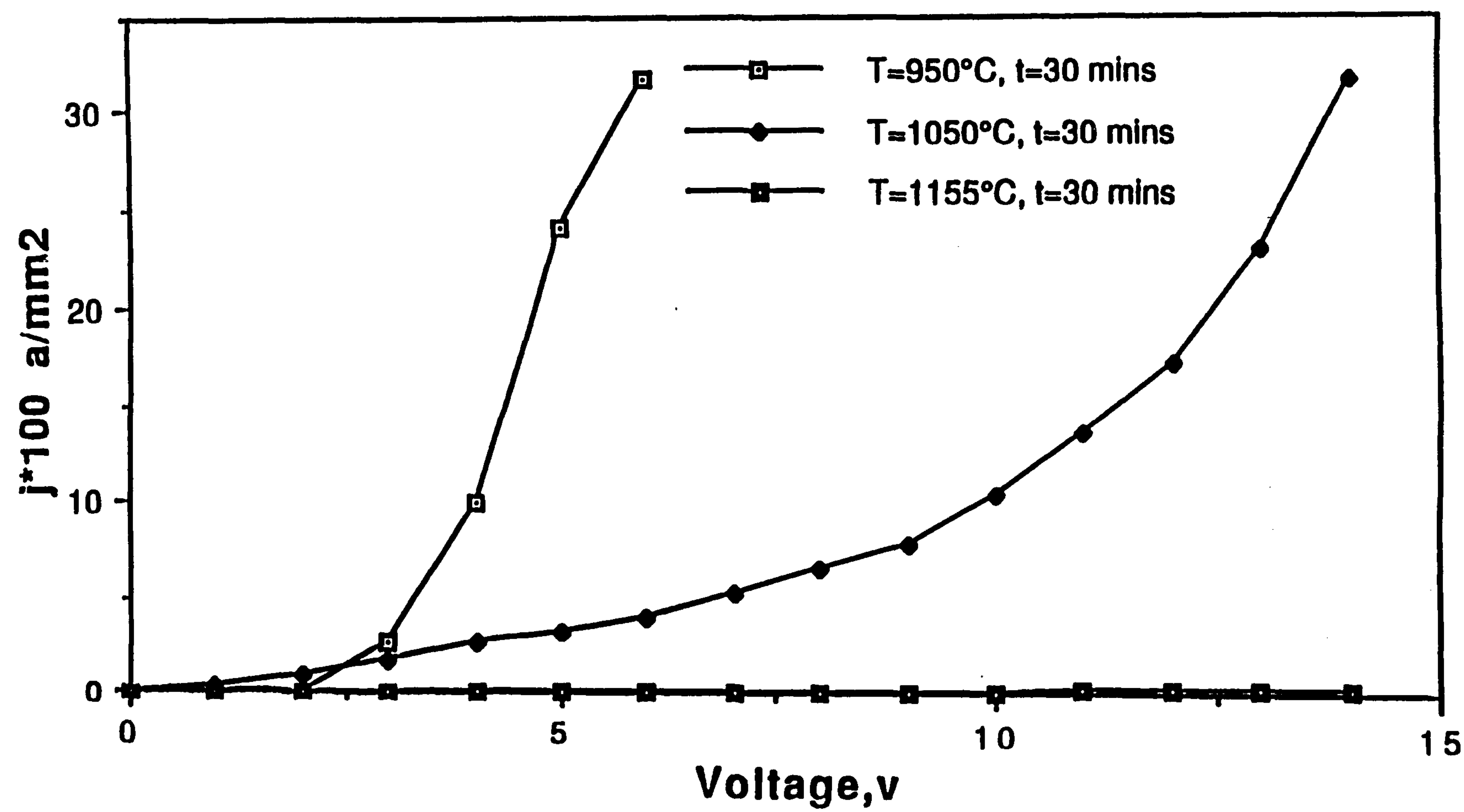

T=950°C, t=30 mins
T=1050°C, t=30 mins
T=1155°C, t=30 mins
j*100 a/mm2
Voltage,v
0
10
20
30
0
5
10
15

Figure 4

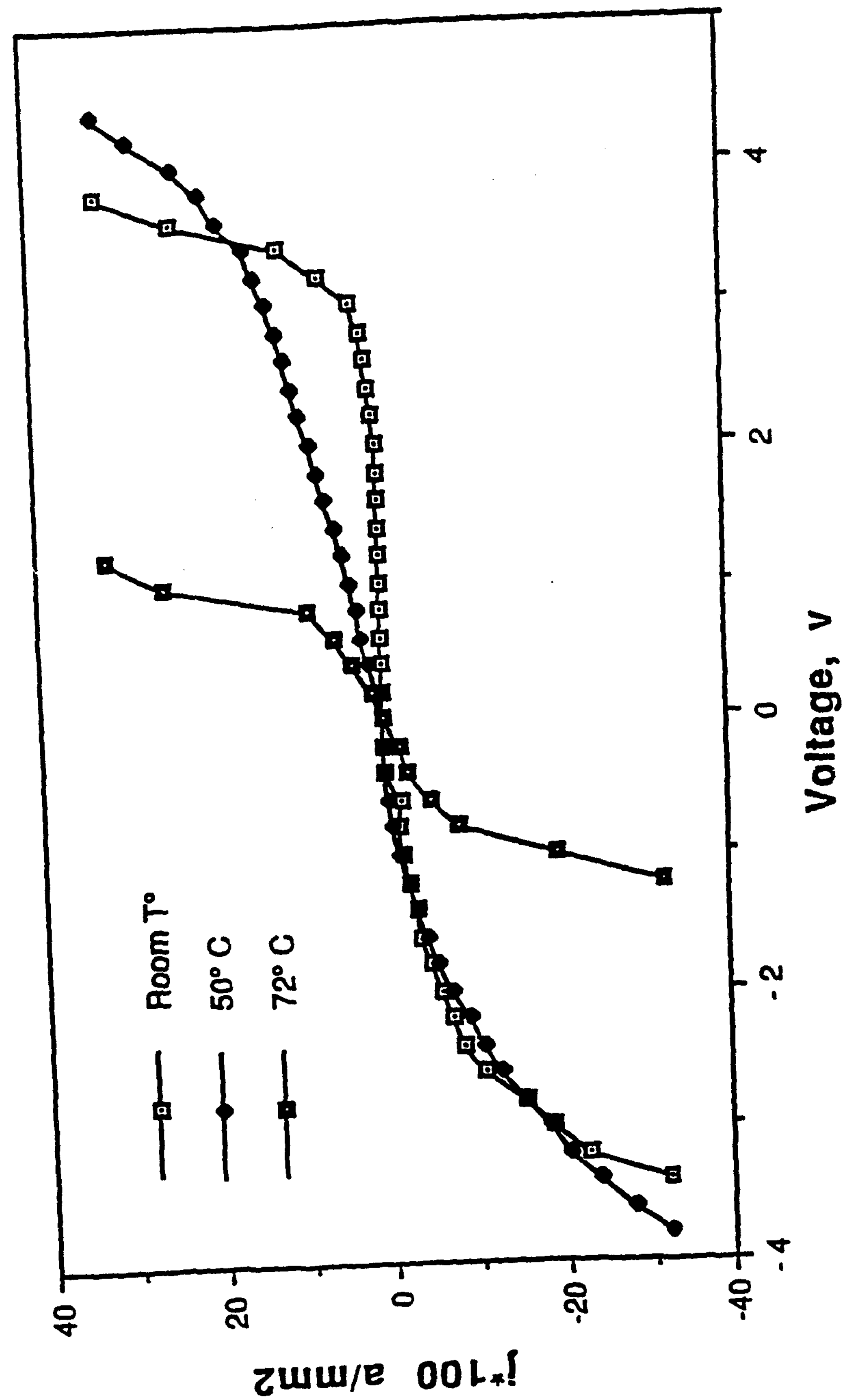


Figure 5

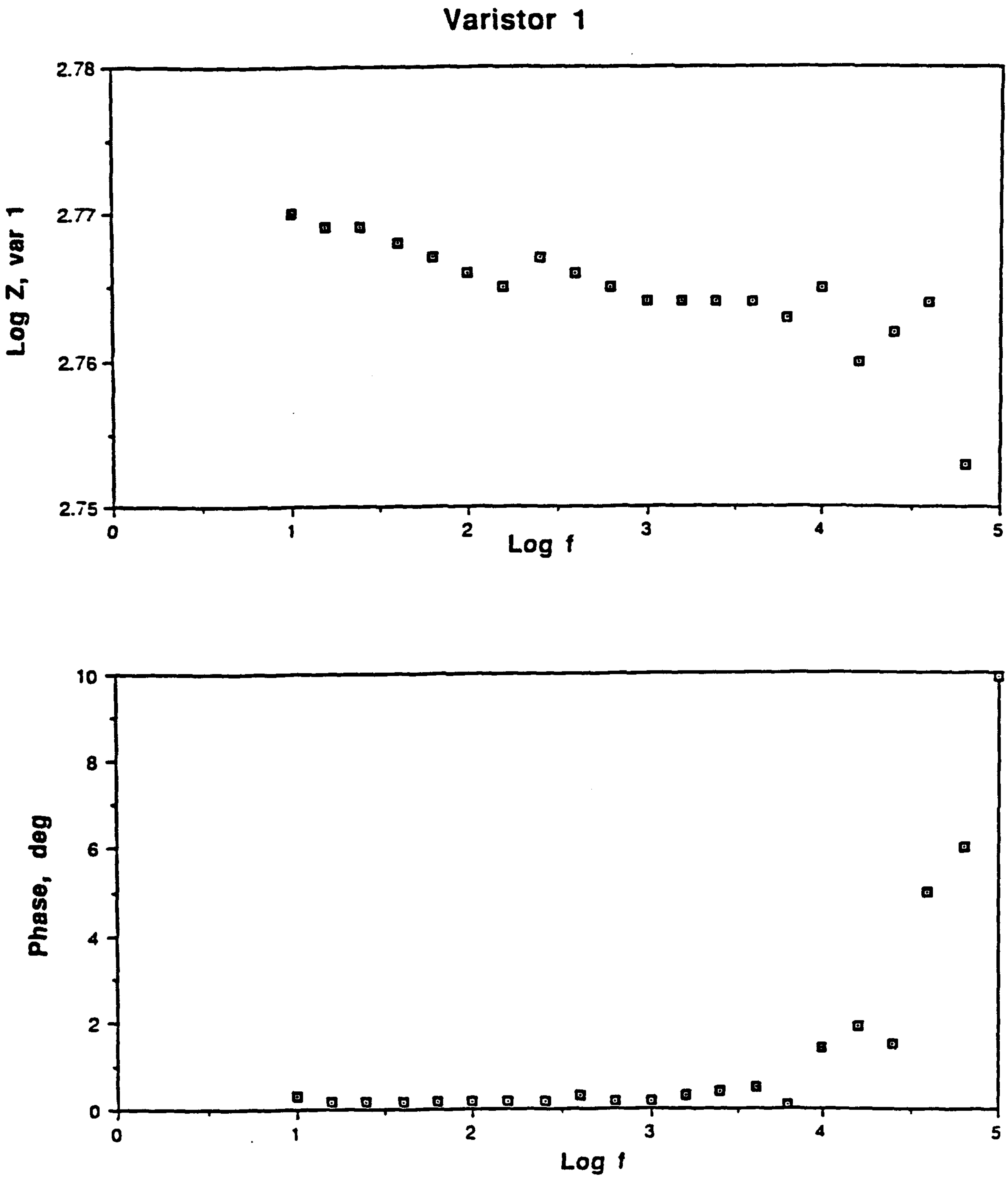

Varistor 1
2.78
2.77
2.76
2.75
Log Z, var 1
0
1
2
3
4
5
Log f
10
8
6
4
2
0
Phase, deg
0
1
2
3
4
5
Log f

Figure 6

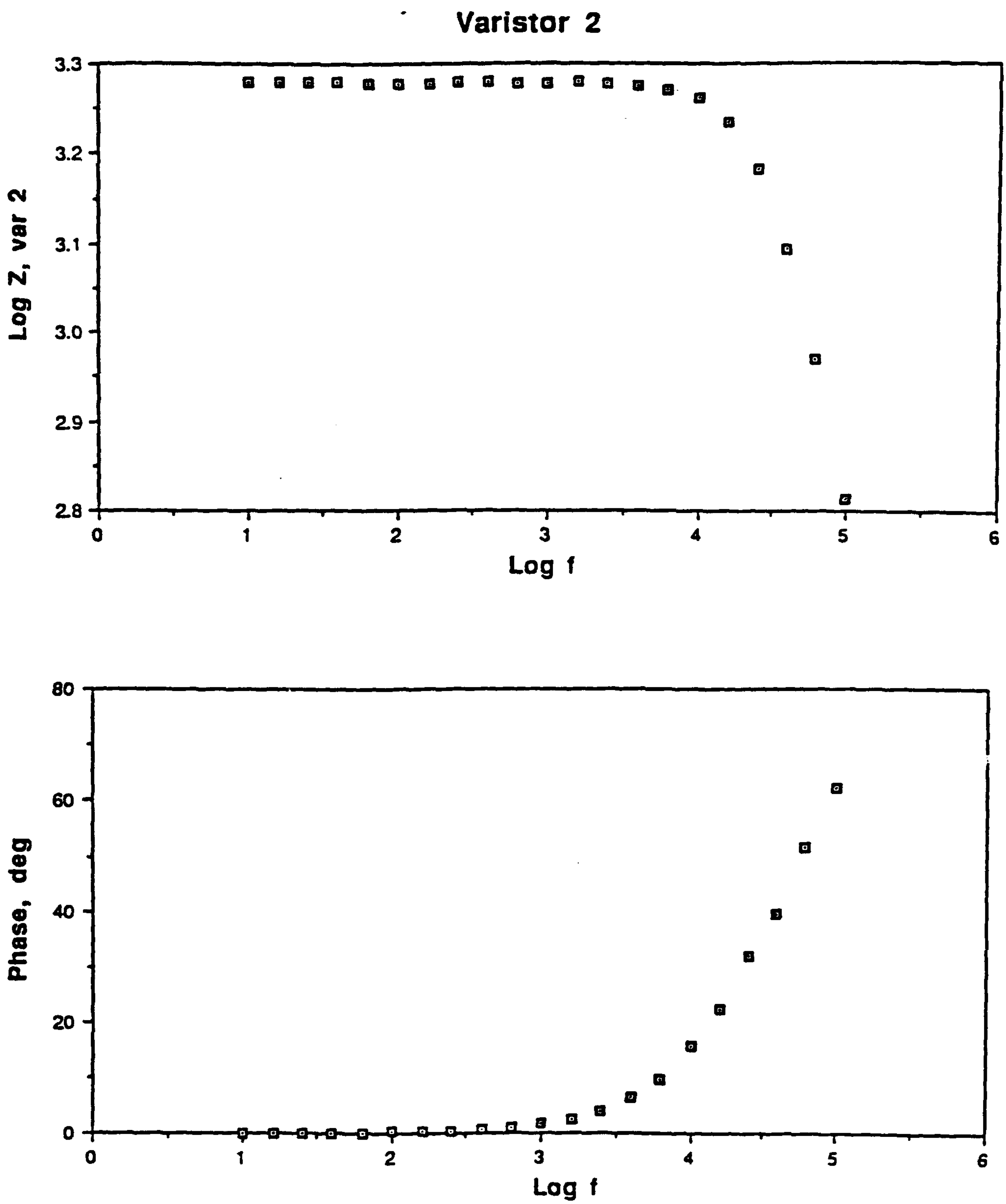
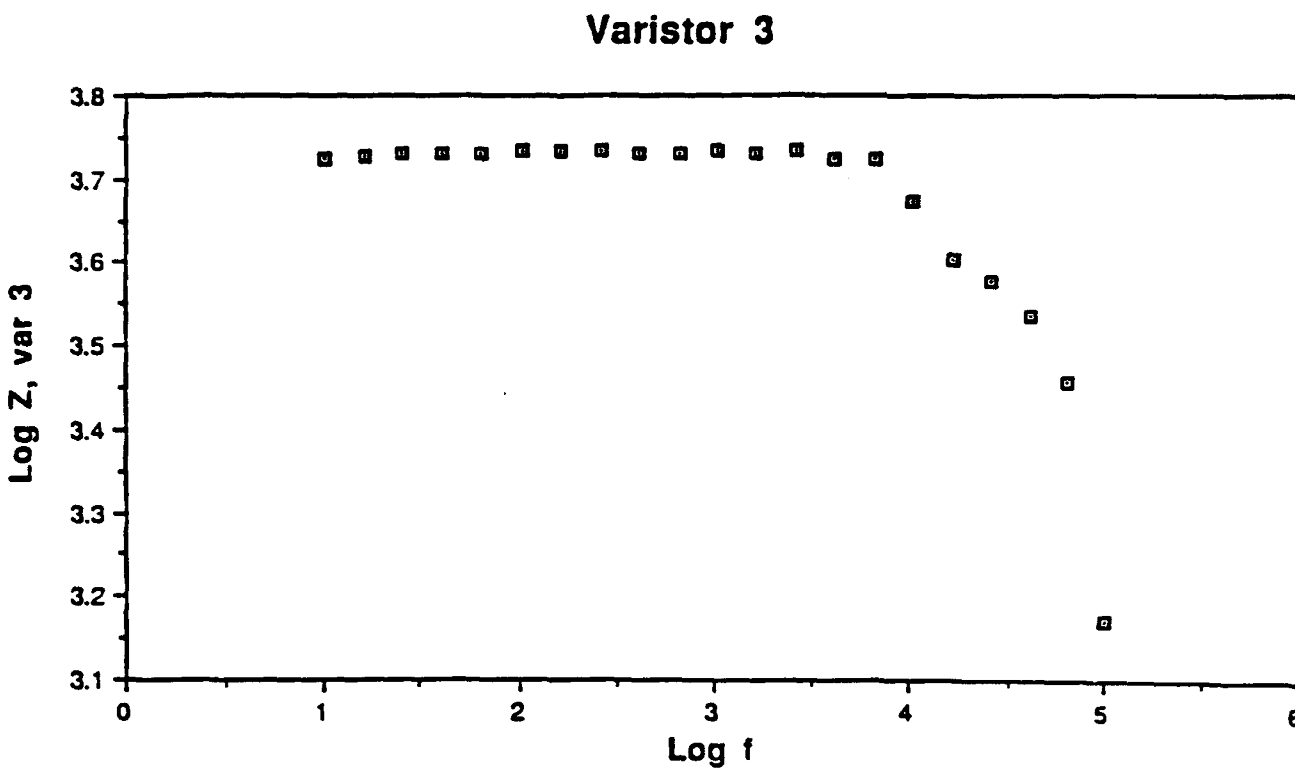
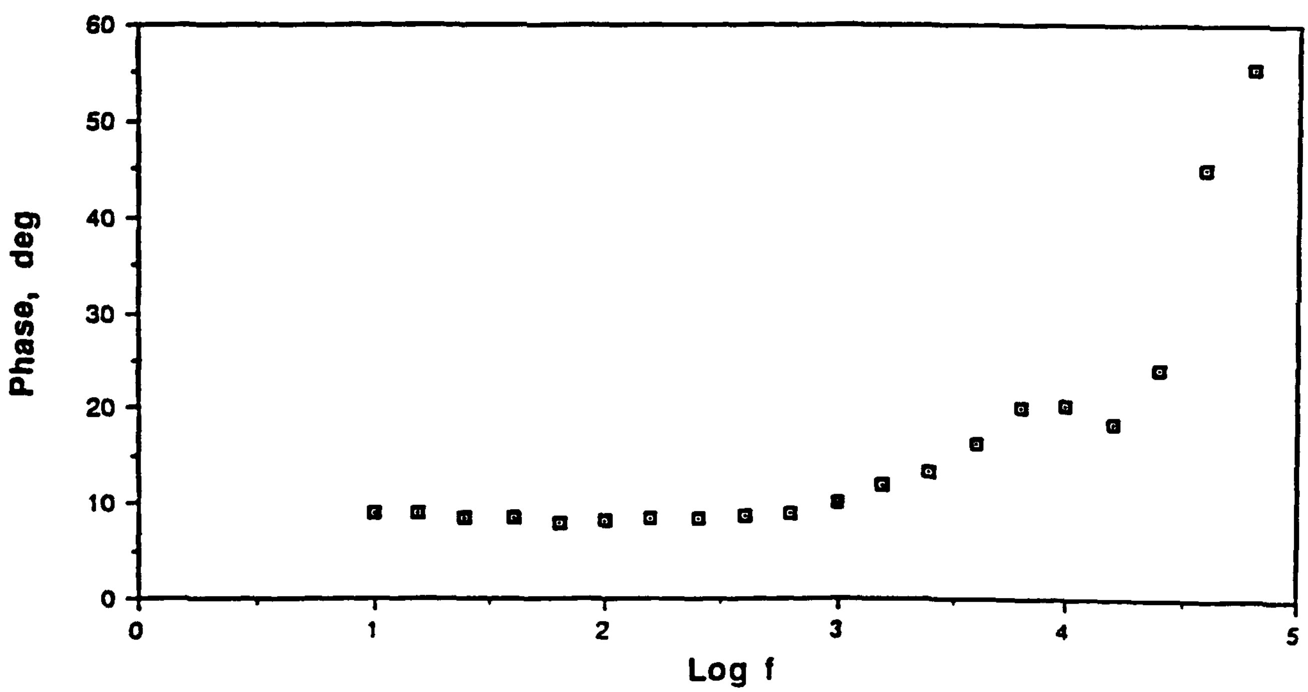

Varistor 2
Log Z, var 2
3.3
3.2
3.1
3.0
2.9
2.8
0
1
2
3
4
5
6
Log f
Phase, deg
80
60
40
20
0
0
1
2
3
4
5
6
Log f

Figure 7



Varistor 3
Log Z, var 3
3.8
3.7
3.6
3.5
3.4
3.3
3.2
3.1
0
1
2
3
4
5
6
Log f



Phase, deg
60
50
40
30
20
10
0
0
1
2
3
4
5
Log f

Figure 8

Table 1. Fabrication Process of ZnO Varistors

1) Milling
2) Calcining
3) Binding
4) Drying
5) Granulating
6) Pressing
7) Sintering
8) Slicing
9) Lapping
10) Polishing
11) Electroding
12) I-V Measurement
13) Packaging
14) I-V Measurement
15) Impedance-Frequency Measurements
16) Turn-on Measurements

Table 2. Milestone Chart and Schedule

A. <u>Basic Effort:</u> Feasibility of 10 MHz Application.

<u>Task Description</u>	<u>Months</u> 0	1	2	3	4	5	6
1) Material Specification and Evaluation		o------	------•				
2) Device Design and Processing	o------	-------	------•				
3) Device Testing Evaluation and of frequency response measurements up to 10 MHz		o------	-------	------•			
4) Analysis of Results and Modelling				o------	-------	------•	
5) Project Reviews and Reporting		o------	-------	------•			

B. <u>Option 1 Effort:</u> 100 MHz Application.

<u>Task Description</u>	<u>Months</u> 0	2	4	6	8	10	12
1) Optimization of Single Barrier Doparts and Diffusions	o------	-------	-------	------•			
2) Surface Passivation and Device			o------	-------	------•		
3) Device Testing Evaluation and of frequency response measurements up to 10 MHz		o------	-------	------•			
4) Project Reviews and Reports			o------	-------	-------	------•	

C. <u>Option 2 Effort:</u> **Frequency Response Limitation and Optimization**

Task Description	Months: 0 2 4 6 8 10 12
1) Optimization of Device Processing	(2) o-----------------------------•
2) Device Design Trade-offs, voltage ratings, energy absorption, and non-linearity vs. conductivity	(0) o-------------------------------------•
3) Limitation to fast switching response	(6) o---------------•
4) Surface passivation and device packaging: Hermetic vs. non-hermetic package	(2) o---•
5) Analysis of Results, Modelling, and Reporting	(2) o-----------------------------------•

∘ Start
• Finish

VIII. Related Research

The principal investigator, Dr. Selim, has been involved with the development of advanced materials and devices for power electronics and integrated circuits for several years. He is currently involved with the development of over-voltage protection devices and MOV electrical transient arrestors for high voltage and low voltage application. It is "hands on" theoretical and experimental research with the aim to process and manufacture electronic materials, ceramics, and devices for IC's applications and to ensure on-shore US capability.

ITS, Inc. has been active in working with several US Eastern Universities (Drexel, Princeton, RPI, and Temple) to establish regional power electronics consortium for collaborative research between industries and universities (Eastern Power Electronics Consortium - EPEC). F.A. Selim is the Director of EPEC.

The principal investigator has special interest in ZnO MOV devices since his involvement with its application at Westinghouse Research Labs in the 1970's Dr. Sendaula of ITS, Inc. is involved with related research on IC's packaging and testing of power electronics Dr. Barsoum, Associate Professor at Drexel University and consultant to ITS, Inc. is also involved with ceramic material processing and characterization.

This work will be performed in coordination with the Materials Science Department of Drexel University in Philadelphia which has considerable activities in electronic ceramic materials and devices.

VIII. Relationship with Future R&D and Potential Commercial Applications

This effort (Phase II) will build on the accomplishment of Phase I and provide a foundation

for commercialization. It is designed to demonstrated the manufacturibility of low voltage ZnO varistor with a single barrier which can be easier to "tailor" for the desired non-linearity and eliminate the highly microstructure dependency in the conventional varistors. This phase will demonstrate the manufacturibility of reproducible and reliable low-cost devices for advanced IC applications such as VHSICs and MIMICs military low voltage applications (~3V) and higher voltage commercial applications (10-12V). After Phase II we plan to commercialize surface-mounted multi-layer chip ZnO varistors with various voltages and energy ratings. The concept proposed in Phase I is anticipated to yield rugged commercial devices.

It is anticipated that this effort will be beneficial for dual use i.e. for all commercial and industrial sectors and Federal Agencies utilizing electronic systems which need pulse suppression and voltage stabilization.

IX. Program Organization and Key Personnel

The development work of this program will be carried out by a team of scientists and engineers who have considerable experience directly connected with this proposed work. The proposed work will be under the direction of F.A. Selim who will have the overall responsibility for bringing the program to a successful and timely conclusion. He will act as the Principal Investigator and will coordinate and perform the tasks and technical activities from material evaluation to device processing and characterization. Dr. Sendaula will have the responsibility of device packaging, testing, rating and evaluation. Dr. Sendaula has several years of experience in material processing, evaluation, and power electronics applications at Temple University and at ITS, Inc. He has a Ph.D. in EE from the University of Connecticut. Dr. Michel Barsoum, Associate Professor of Materials Sciences at

Drexel University, Philadelphia will work as a consultant for ITS, Inc. in device modelling. He will model device results and study the non-linearity of the devices at different current densities. Dr. Barsoum has a Ph.D. in Materials Sciences from MIT, Massachusetts.

There will be no conflict between the proposed program and any other or anticipated contract. F.A. Selim will devote the majority of his activities to work on the program for twenty-four months.

A biographical sketch of the Principal Investigator is shown on the following page.